| AMENDMENT TRANSMITTAL LETTER (Large Entity) | | | Docket No. |
|---|---|---|---|
| Applicant(s): DONALD W. MACINTYRE | | | MCSP-101 |
| Serial No. 09/045,507 | Filing Date March 20, 1998 | Examiner D. Willie | Group Art Unit 2814 |



Invention: CHIP SCALE PACKAGES

TO THE ASSISTANT COMMISSIONER FOR PATENTS:

Transmitted herewith is an amendment in the above-identified application.

The fee has been calculated and is transmitted as shown below.

CLAIMS AS AMENDED

| | CLAIMS REMAINING AFTER AMENDMENT | | HIGHEST # PREV. PAID FOR | | NUMBER EXTRA CLAIMS PRESENT | RATE | ADDITIONAL FEE |
|---|---|---|---|---|---|---|---|
| TOTAL CLAIMS | 10 | - | 20 | = | 0 | x $18.00 | $0.00 |
| INDEP. CLAIMS | 3 | - | 3 | = | 0 | x $80.00 | $0.00 |
| Multiple Dependent Claims (check if applicable) ☐ | | | | | | | $0.00 |
| TOTAL ADDITIONAL FEE FOR THIS AMENDMENT | | | | | | | $0.00 |

☐ No additional fee is required for amendment.

☐ Please charge Deposit Account No. in the amount of
A duplicate copy of this sheet is enclosed.

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☒ The Commissioner is hereby authorized to charge payment of the following fees associated with this communication or credit any overpayment to Deposit Account No. **50-1703**
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- ☒ Any additional filing fees required under 37 C.F.R. 1.16.
- ☐ Any patent application processing fees under 37 CFR 1.17.

Dated: **May 16, 2001**

*Signature*

**Michael J. Pollock**
**Reg. No. 29,098**

I certify that this document and fee is being deposited on May 16, 2001 with the U.S. Postal Service as first class mail under 37 C.F.R. 1.8 and is addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231

CC:

**Chianti Appling**
*Typed or Printed Name of Person Mailing Correspondence*

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

DONALD M. MACINTYRE

Application No.: 09/045,507

Filed: March 20, 1998

For: CHIP SCALE PACKAGES

Group Art Unit: 2814

Examiner: D. Willie

**RESPONSE TO OFFICE ACTION MAILED NOVEMBER 21, 2000**

121 Spear Street, Suite 290
San Francisco, CA 94105
(415) 512-1312

**CERTIFICATE OF MAILING**

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope, addressed to: Commissioner for Patents, Washington, DC 20231 on May 16, 2001.

STALLMAN & POLLOCK LLP

Dated: 5/16/01 By: _____
Chiahti Appling

Commissioner for Patents
Washington, D.C. 20231

Sir:

Please amend the above-identified application as follows:

IN THE CLAIMS

Please cancel claims 18-38 and add the following new claims:

--39. (New) A semiconductor integrated circuit structure comprising:

a semiconductor wafer substrate that includes a plurality of semiconductor integrated circuit die formed in an upper surface of said wafer substrate;

for each semiconductor integrated circuit die, a plurality of conductive die bond pads formed on an upper surface of said integrated circuit die;

a glass sheet having a plurality of holes formed therethrough from an upper surface of the [illegible] lower surface of the glass sheet